A Novel Configuration for $1:N$ Multiport Power Dividers Using Series/Parallel Transmission-Line Division and a Polyimide/Alumina–Ceramic Structure for HPA Module Implementation

Masashi Nakatsugawa, *Member, IEEE,* and Kenjiro Nishikawa, *Member, IEEE*

***Abstract*—A novel configuration for $1:N$ multiport power dividers using series and parallel division of the transmission lines with a polyimide/alumina–ceramic structure is proposed and successfully demonstrated. Since these circuits need only line divisions and mode transitions to function as power dividers, they inherently possess an extremely flat frequency response. The polyimide/alumina–ceramic substrate suits the three-dimensional arrangement of various kinds of transmission lines and their transitions. It is also useful in implementing high-power-amplifier multichip modules because the alumina substrate can hold all active devices or monolithic microwave integrated circuits and provides convenient interfaces between them and the power dividers. The line divisions and mode transitions are analyzed by a commercial electromagnetic simulator. Two types of $1:4$ power dividers, which are series/parallel and parallel/series configurations, are fabricated. No peculiar resonance was observed over the frequency range of 1–8 GHz. The amplitude deviation over this range was less than 3.2 dB.**

***Index Terms*—Alumina, multilayer, parallel division, polyimide, series division, transformation, transmission line.**

I. Introduction

TO REALIZE the development of advanced wireless communication systems, RF circuits with broad-band or multiband capability are more important than ever before. In order to satisfy the high data-rate transmission requirement with many channels, the bandwidths of the future wireless communication systems should be drastically increased. Moreover, new systems under development like software defined radios (SDRs) [1] require an especially broad frequency range. SDRs can operate as several kinds of wireless communication systems simply by replacing their signal processing software. This changeability can be realized only if the hardware supports all of the frequency bands used by each system. For these reasons, increasing the frequency range offered by RF components is becoming a critical goal.

High-power amplifier (HPA) modules are essential components to construct any kinds of wireless communication systems. Their improvement will facilitate reductions in the cost, size, and power consumption of the systems. Fabricating amplifier modules with solid-state devices is one attractive approach to miniaturizing the components as well. However, the maximum available output power is constrained by the performance of each device. In order to increase the total output of the power-amplifier modules, the input power should be divided among the unit amplifiers used. After which, each stream should be amplified and effectively recombined.

Wilkinson dividers, branch-line hybrids, and directional couplers are frequently used as power-dividing and power-combining components in conventional HPA modules [2]–[5]. A common feature is that they consist of quarter-wavelength transmission lines or equivalent impedance-transforming networks. Although they have an interesting response under impedance transformation, their passband width is limited. In order to eliminate this constraint, the dividers must usually have more transmission lines so as to prevent any drastic change in the characteristic impedance of the lines. This expands the total size of the power dividers and increases the insertion losses.

In this paper, we propose a novel configuration to realize power dividers. The configuration consists of series and parallel division of the transmission lines fabricated on a polyimide/alumina–ceramic multilayer structure. It also reduces unwanted resonance at the power divisions and line-type transitions. This improves the frequency response and increases the available frequency range. The polyimide/alumina–ceramic structure is suitable to build various types of transmission lines and their transitions and, thus, simplifies the power-divider layout. The characteristics of the divisions and transitions were examined by a commercial electromagnetic simulator. With the proposed configuration, extremely broad frequency-band power dividers are obtained.

II. Conventional Structure

Some conventional configurations for the $1:N$ power dividers are shown in this section. Specifically, $1:4$ power dividers are discussed. Fig. 1(a) and (b) shows the type-A and type-B configurations for $1:4$ Wilkinson power dividers, respectively. In type-A, the power fed to the input port of the power divider is divided into four and delivered to each of the output ports. In order to maintain impedance matching at the circuit interfaces, all of the ports should have standard impedance $Z_{\rm o}$, which is usually chosen as 50 Ω. The quarter-wavelength transmission lines are used for impedance

Manuscript received February 1, 2000; revised November 1, 2000.

The authors are with the Wireless Systems Innovation Laboratory, NTT Network Innovation Laboratories, Yokosuka, Kanagawa 239-0847, Japan.

Publisher Item Identifier S 0018-9480(01)04440-4.

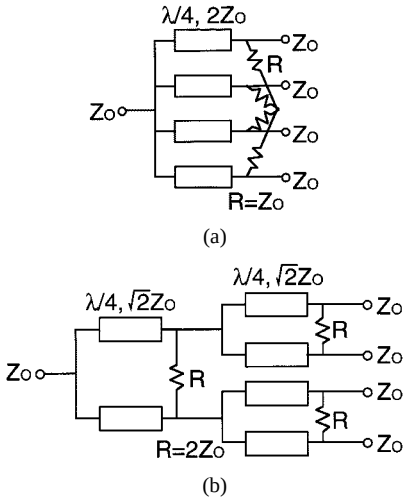


Fig. 1. (a) Type-A Wilkinson divider. (b) Type-B Wilkinson divider.

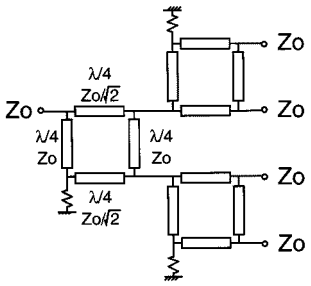


Fig. 2. $1:4$ power divider using branch-line hybrids.

transformation. As is well known for a quarter-wavelength line, characteristic impedance Z is related to input impedance $Z_{\rm in}$ and output impedance $Z_{\rm out}$ as shown in the following:

$$Z = \sqrt{Z_{\rm in} \cdot Z_{\rm out}}. \tag{1}$$

Hence, the transmission lines in type A should have a characteristic impedance of $2Z_{\rm o}$.

Type B is an alternative that avoids drastic changes in the characteristic impedance of the transmission lines. Two $1:2$ dividers are cascaded to build the $1:4$ divider. As the change in impedance is more moderate than that in type A, $\sqrt{2}Z_{\rm o}$ transmission lines can be used in this configuration. The drawback of type B is that it uses more transmission lines than type A. This can increase the insertion losses and the occupied circuit area.

Fig. 2 shows another configuration of the $1:4$ power divider. This is composed of three branch-line hybrids. Since each of the branch-line hybrids contains two pairs of quarter-wavelength transmission lines, the area can easily become larger than that of the Wilkinson divider. In addition, the bandwidth of this power divider is the narrowest among the examples.

The weakness of these three circuits is caused by the use of the quarter-wavelength transmission lines. Eliminating the use of quarter-wavelength transmission lines can improve the performance and reduce the size of the power dividers. In the following section, series and parallel divisions of the transmission lines and their application to power dividers will be described.

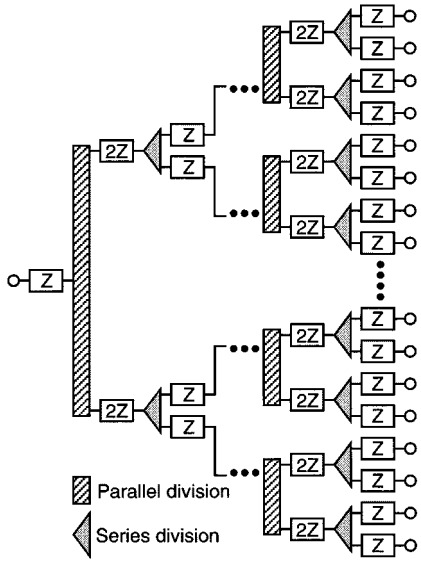


Fig. 3. Generalized configuration of the series/parallel-division power divider.

III. Series/Parallel-Division Power Dividers with Polyimide/Alumina–Ceramic Structure

Fig. 3 shows the generalized configuration of the series/parallel-division power divider. A fundamental unit of this power divider is the cascade connection of a series and a parallel division of the transmission line. This makes a four-port power divider. The series division halves the port impedance, while the parallel one doubles it. Hence, the circuits whose series signal path contains the same number of series and parallel divisions have the same output impedance as that of the input. When n units are connected in series, the number of ports $N_{\rm p}$ is given by the following:

$$N_{\rm p} = 4^n. \tag{2}$$

These line lengths need not to be a quarter-wavelength. Moreover, this configuration does not impose any frequency response limit because it employs only the line-type transitions of the transmission lines. Therefore, the frequency performance is theoretically flat over the entire frequency range.

Fig. 4(a) and (b) shows two examples of the series/parallel-division power divider. In Fig. 4(a), the power is first divided in parallel and series divisions follow. The impedance combination of this arrangement is 50–100–50 Ω. This configuration is suitable if the fabrication process can accurately fabricate 100-Ω lines. Fig. 4(b) shows the 50–25–50-Ω configuration. This is favorable when precise 25-Ω lines can be produced.

A. Series Division of the Transmission Lines

Series division of the transmission lines halves the impedance. Examples for the slotline and stripline arrangements are shown in Fig. 5(a) and (b), respectively. Intuitively, the mechanism of this division can be explained as follows. We can assume the existence of a symmetrically distributed electric field between the two conductors forming the line. When the third conductor is inserted exactly between these two conductors, the strength of the overall electric field is not affected by this physical change. The voltage impressed

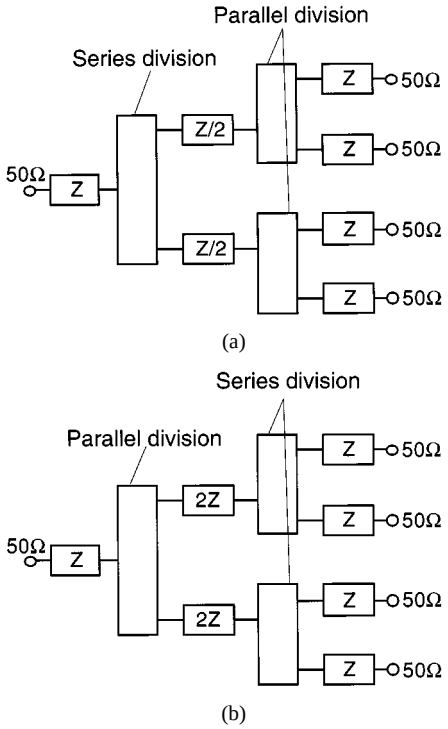


Fig. 4. Examples of the series/parallel-division power dividers. (a) 50–100–50 Ω. (b) 50–25–50 Ω.

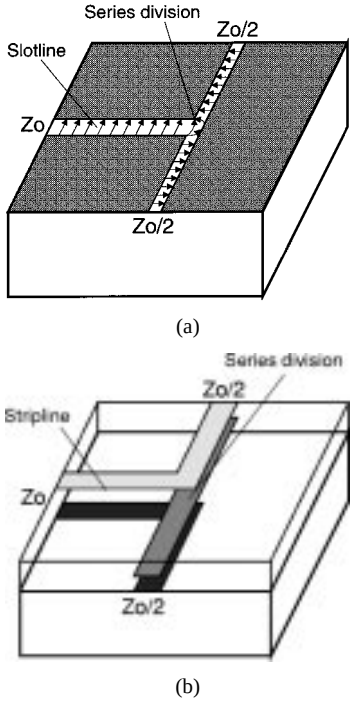


Fig. 5. Series division of the transmission line. (a) Slotline. (b) Stripline.

on one of the conductors and the third one is one-half of the original. However, the condition for the current remains the same as before. As a result, the impedance of the divided part is one-half that of the original line. Consequently, series division of the transmission line can halve the impedance.

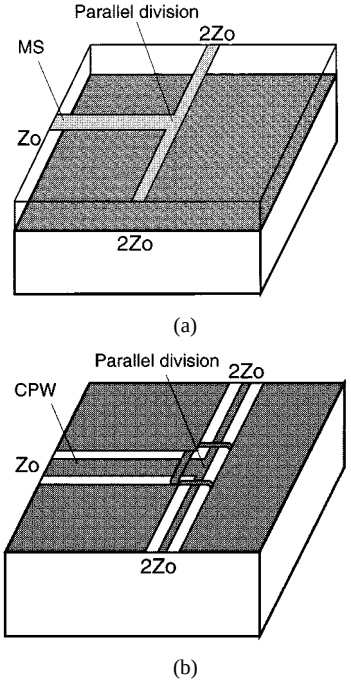


Fig. 6. Parallel division of the transmission line. (a) MS. (b) CPW.

B. Parallel Division of the Transmission Lines

Parallel division of the transmission lines doubles the impedance. This is normally used for simple line divisions. The mechanism of the impedance change can be explained by analogy to the parallel connection of two passive circuit elements. In order to obtain total impedance of Z, the impedance should be $2Z$ if two elements are connected in parallel. Similarly, the characteristic impedance of the transmission lines, which are connected in parallel, should be $2Z$ to yield the same impedance as the transmission line whose characteristic impedance is Z. Conversely, the output impedance would be twice the input impedance if one transmission line is divided into two. Fig. 6(a) and (b) shows examples of these types of divisions. The former shows the microstrip line (MS), and the latter shows the coplanar waveguide (CPW).

C. Utilization of Three-dimensional Properties of the Polyimide/Alumina–Ceramic Structure

Many reports have described the flexibility offered by the multilayer structure in fabricating transmission lines [6], [7]. The introduction of the three-dimensional structure helps to increase the freedom in arranging the various kinds of transmission lines and their combinations. The authors previously reported a series/parallel-division power divider fabricated with a combination of CPWs and slotlines, both of which are a planar structure [8]. However, using the three-dimensional structure with series and parallel divisions has not been reported to date. Combining the advantages of the three-dimensional structure with those of the series/parallel-division power dividers optimizes the construction of transmission-line transitions, which reduces ruffles in the electromagnetic fields at the transitions. This improves the overall performance of the dividers.

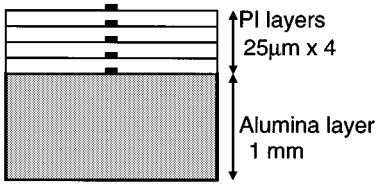
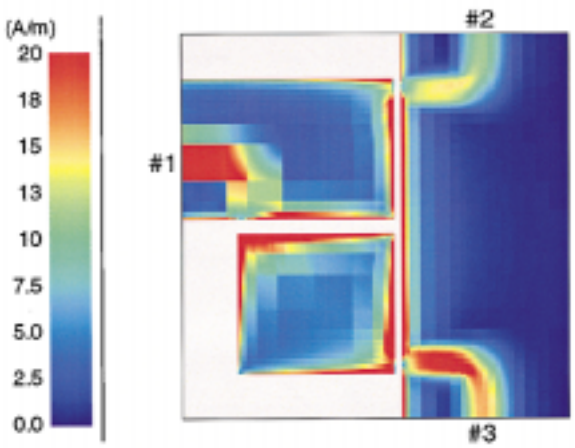
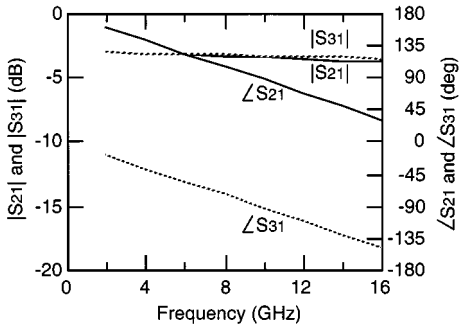


Fig. 7. Cross section of the substrate.



(a)



(b)

Fig. 8. Simulated results. (a) Simulated current density of the divider. (b) Simulated performance of the divider.

A cross section of the basic polyimide/alumina–ceramic substrate [9] is shown in Fig. 7. The base–substrate is 1-mm-thick alumina. The polyimide part is composed of four layers of a 25-μm-thick polyimide film. All of the lines are made of copper, whose thickness is 5 μm. This structure enables us to realize low-loss components. Moreover, HPA modules can be constructed with this structure easily because the alumina substrate is suitable for holding active devices or monolithic microwave integrated circuits (MMICs).

D. Electromagnetic Simulation of the Divider

Divider performance was analyzed by using the commercial electromagnetic simulator ***em*** of Sonnet Software Inc., Liverpool, NY. Visualized current density and frequency responses are shown in Fig. 8(a) and (b). The current is mostly concentrated at the points of mode transitions and is distributed evenly along the slotlines' gap, both before and after the line divisions. The calculated results indicate that the derived current of the line, which is originally connected to the signal line of the MS (S_{31}), was slightly larger than that connected to the ground (S_{21}). The phase difference between these two output signals was exactly 180°, which is extremely useful when realizing baluns and antiphase dividers.

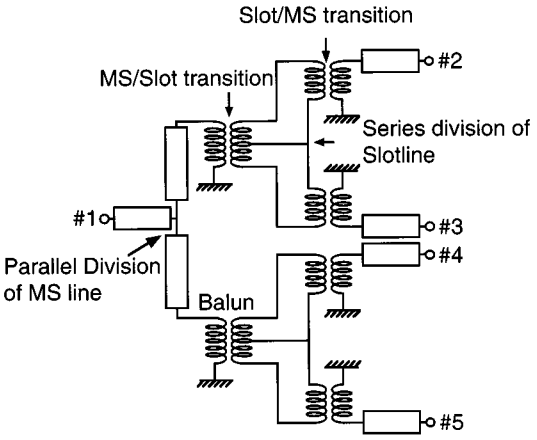


Fig. 9. Equivalent circuit of the parallel(MS)/series(slot) divider.

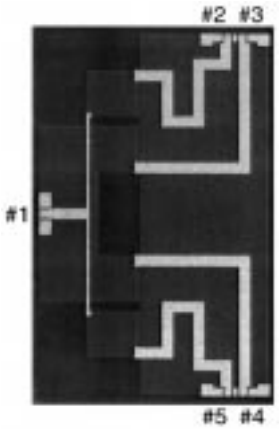


Fig. 10. Parallel(MS)/series(slot) divider.

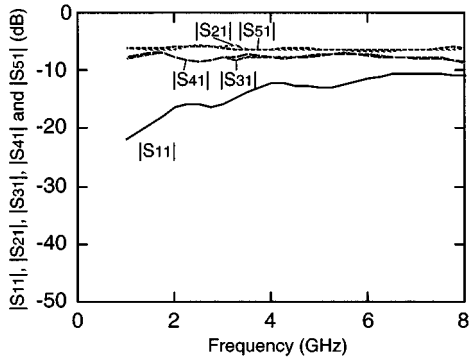


Fig. 11. Performance of the parallel(MS)/series(slot) divider.

IV. Experimental Results

A. Parallel(MS)/Series(Slot) Dividers

Fig. 9 shows the equivalent circuit of the parallel(MS)/series(slot) divider. The input port for this divider is an MS line divided into two parallel lines. Each of the lines are transformed into slotlines and divided into two in series. The slotlines are

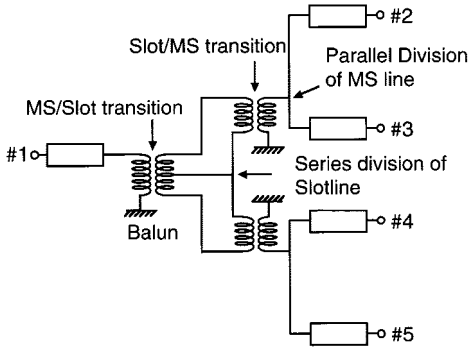


Fig. 12. Equivalent circuit of the series(slot)/parallel(MS) divider.

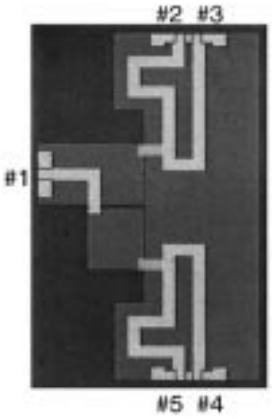


Fig. 13. Photograph of the series(slot)/parallel(MS) divider.

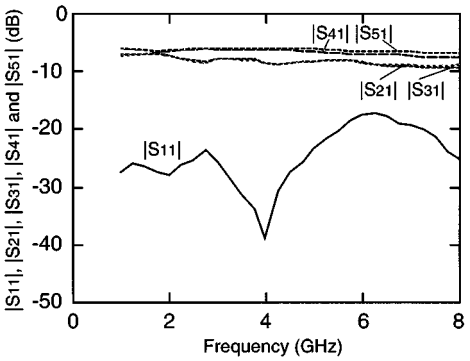


Fig. 14. Performance of the series(slot)/parallel(MS) divider.

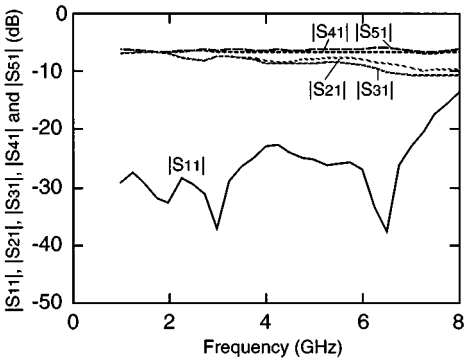


Fig. 15. Performance of the series(slot)/ parallel(CPW) divider.

again transformed into MSs, and divided into two. Thus, this structure has 50–100–50-Ω combinations, which are parallel/series divisions.

Fig. 10 shows a photograph of the parallel(MS)/series(slot) divider. The input port is located at the left-hand-side edge of the substrate, and the two output ports are on the top and bottom sides.

Fig. 11 shows the performance of the parallel(MS)/series(slot) divider. Input return loss was more than 11 dB over the frequency range from 1 to 8 GHz. S_{21} ranged from -5.5 to -6.7 dB, S_{31} from -6.9 to -8.6 dB, S_{41} from -6.8 to -8.3 dB and S_{51} from -5.7 to -6.5 dB. The performance was quite flat over the measured range. At any frequency, the insertion losses of S_{21} and S_{51} were smaller than those of S_{31} or S_{41}.

B. Series(Slot)/Parallel(MS) Dividers

Fig. 12 shows the equivalent circuit of the series(slot)/parallel(MS) divider. Although the input port is an MS, it is immediately transformed into a slotline, which is divided into two in series. Each of the divided lines are transformed into MS lines and divided into two in parallel. Thus, this structure offers 50–25–50 Ω, which are series/parallel divisions.

Fig. 13 shows a photograph of the series(slot)/parallel(MS) divider. The input port is located at the left-hand-side edge of the substrate, and the two output ports are on the top and bottom sides. The line sizes are exactly the same as those simulated, which are shown in Fig. 8(a).

Fig. 14 shows the performance of the series(slot)/parallel(MS) divider. Input return loss was more than 18 dB over the frequency range from 1 to 8 GHz. S_{21} ranged from -6.9 to -8.8 dB, S_{31} from -6.7 to -9.2 dB, S_{41} from -6.0 to -7.4 dB and S_{51} from -5.9 to -6.7 dB. The performance was quite flat over the measured frequency range. The insertion losses of S_{21} and S_{31} were larger than those of S_{41} or S_{51}

C. Comparison Between Series(slot)/Parallel(MS) with Series(Slot)/Parallel(CPW) Dividers

In order to compare the proposed divider to a conventional one, the series(slot)/ parallel(CPW) divider was fabricated. The only difference from the one described in the previous section is that it uses a CPW instead of an MS.

Fig. 15 shows the performance of the series(slot)/parallel(CPW) divider. Input return loss was more than 13 dB over the frequency range from 1 to 8 GHz. S_{21} ranged from -6.8 to -9.9 dB, S_{31} from -6.8 to -10.9 dB, S_{41} from -6.2 to -7.1 dB and S_{51} from -6.1 to -6.6 dB. The performance was flat over the measured range. The insertion losses of S_{21} and S_{31} were larger than those of S_{41} or S_{51}.

Fig. 16 shows a comparison between slot/MS and slot/CPW configurations. The loss of the slot/CPW type is larger than that of the slot/MS.

V. Discussions

The fabricated MS/slot and slot/MS exhibit excellent performance especially with regard to the flatness of the frequency response over the measured frequency range. The common tendency is that the insertion losses of two of the outputs (connected to the signal line of the unbalanced line) were larger than those other two (connected to the ground plane). The ports

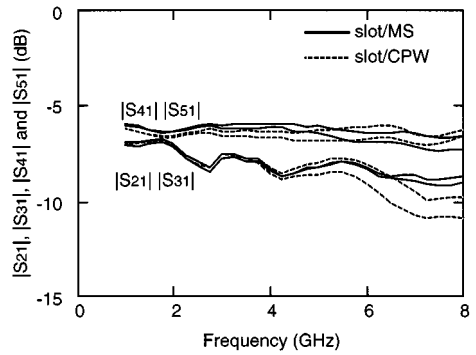


Fig. 16. Comparison between slot/MS and conventional slot/CPW performances.

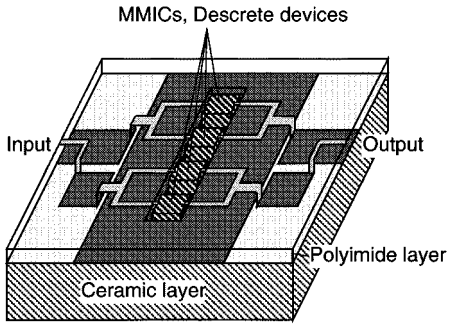


Fig. 17. Conceptual view of a substrate used as an MCM module.

that had larger loss received less power because of the imbalance seen within the power dividers, especially in the high-frequency range. This imbalance, measured as the insertion loss, must be added to the conductor loss of the transmission lines of the power dividers. This deteriorated the loss performance of the two outputs. The performance can be improved by making all output levels at the ports the same. To do so, further optimization in designing the dividers' layouts is needed. Although the imbalance should be corrected to obtain equal outputs, the results agree with the simulations. This presumably happened because of imperfection in the mode transition from/to unbalance to/from balance mode. An effective solution may be to lengthen the balanced line part to ensure more complete mode transition.

When MS/slot and slot/MS circuit patterns were designed, we encountered difficulties in designing low-impedance slotlines using the pattern layout rules for this substrate. Developing fine fabrication processes is the key to achieving more freedom in selecting the line impedances and types. The high-impedance MS lines turn out to have narrow signal lines, which deteriorate loss performance. In order to overcome this, optimization of the polyimide-layer thickness should be considered.

Concerning the difference between the slot/CPW and the slot/MS configurations, the signal lines for the CPW should be narrower than those for MS to reach 50 Ω. Consequently, the increase in the conductor loss becomes noticeable and degrades total performance. In addition, the physical layout restriction caused by the CPW use requires additional area and length for the transitions because the CPW needs gaps between signal and ground planes. Therefore, MS and slotlines are more neatly connected than the CPW and slotlines. This reduces unwanted disturbance of the electromagnetic field at mode transitions. Thus, MS configurations yield better flatness than CPW ones.

VI. Using the Substrate as an HPA Module

Fig. 17 shows a conceptual view of this substrate used as an HPA module. The power dividers are fabricated in the polyimide layer, and all MMICs and/or discrete devices are mounted on the alumina–ceramic substrate [10]. The alumina can be replaced AlN, which has excellent heat radiation performance to overcome thermal breakdown of the active devices, if thermal radiation is a critical issue. Moreover, a Class-B push–pull amplifier can be implemented if the proposed power dividers' antiphase characteristics are effectively exploited. Furthermore, this $1:N$ power divider may be used for the feeding network of array antennas. These characteristics mean that the proposed structure well suits HPA module realization.

VII. Conclusion

A novel configuration for $1:N$ multiport power dividers has been proposed and $1:4$ power dividers with polyimide/alumina–ceramic structure have been demonstrated in this paper. Two types of impedance combinations, i.e., 50–100–50 Ω (parallel/series) and 50–25–50 Ω (series/parallel) were discussed. Both have promising power-dividing performance. The latter has been compared to the slot/CPW configuration. The use of the proposed configuration in realizing HPA modules has been described. Thus, the proposed configuration is suitable for constructing HPA MCMs.

Acknowledgment

The authors would like to thank Dr. H. Mizuno, NTT Network Innovation Laboratories, Yokosuka, Japan, Dr. S. Kubota, NTT Science and Core Technology Laboratory Group, Atsugi, Japan, and K. Araki, NTT Network Innovation Laboratories, Yokosuka, Japan, for their encouragement during this paper's preparation. The authors are grateful to Dr. M. Muraguchi, NTT Electronics Corporation, Atsugi, Japan, for fruitful discussions and suggestions. The authors also wish to thank Prof. M. Aikawa, Saga University, Saga, Japan, Dr. T. Tokumitsu, Fujitsu Quantum Devices Limited, Nakakoma, Japan, and Dr. K. Kamogawa, NTT DoCoMo Inc., Yokosuka, Japan, for their invaluable comments on three-dimensional microwave circuits technologies.

References

[1] J. Mitola, III, *Software Radio Architecture*. New York: Wiley, 2000.
[2] E. J. Wilkinson, "An n-way hybrid power divider," *IRE Trans. Microwave Theory Tech.*, vol. MTT-8, pp. 116–118, Jan. 1960.
[3] D. Antsos, R. Crist, and L. Sukamto, "A novel Wilkinson power divider with predictable performance at K- and Ka-band," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1994, pp. 907–910.
[4] H. Ashoka, "Practical realisation of difficult microstrip line hybrid couplers and power dividers," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1992, pp. 273–276.
[5] S. J. Parisi, "180° lumped element hybrid," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1989, pp. 1243–1246.
[6] T. Tokumitsu, T. Hiraoka, H. Nakamoto, and M. Aikawa, "Multilayer MMIC using a $3\ \mu\text{m} \times N$-layer dielectric film structure," *IEICE Trans. Electron.*, vol. E75-C, no. 6, pp. 698–706, June 1992.

[7] M. Hirano, K. Nishikawa, I. Toyoda, S. Aoyama, S. Sugitani, and K. Yamasaki, "Three-dimensional passive circuit technology for ultra-compact MMIC's," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 2845–2850, Dec. 1995.
[8] M. Nakatsugawa and M. Muraguchi, "A 26 GHz-band uniplanar MMIC amplifier using series and parallel divider/combiner combination technique," (in Japanese), IEICE, Tokyo, Japan, Tech. Rep. MW90–138, vol. 90, Jan. 1991.
[9] R. Kambe, R. Imai, T. Takada, M. Arakawa, and M. Kuroda, "MCM substrate with high capacitance," *IEEE. Trans. Comp., Packag., Manufact. Technol. B*, vol. 18, pp. 23–27, Feb. 1995.
[10] M. Nakatsugawa, A. Kanda, H. Okazaki, K. Nishikawa, and M. Muraguchi, "Line-loss and size reduction techniques for millimeter-wave RF front-end boards by using a polyimide/alumina–ceramic multilayer configuration," *IEEE. Trans. Microwave Theory Tech.*, vol. 45, pp. 2308–2315, Dec. 1997.

Masashi Nakatsugawa (S'97–M'99) was born in Hamamatsu, Japan, in 1963. He received the B.E. degree in electronics and communication engineering and the M.E. degree in electrical engineering from Waseda University, Tokyo, Japan, in 1987 and 1989, respectively, and the M.S. degree in electrical engineering from the California Institute of Technology, Pasadena, in 1999.

In 1989, he joined NTT Radio Communication Systems Laboratories, Yokosuka, Japan. From 1989 to 1997, he was involved in the research and development of MMICs and packaging technologies. In 1998, he was a Research Assistant at the California Institute of Technology. He is currently a Senior Research Engineer at NTT Network Innovation Laboratories, Yokosuka, Japan, where he performs research on software radio architecture.

Mr. Nakatsugawa is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan and the Japan Society of Applied Physics. He was the recipient of the 1996 Young Engineer Award presented by IEICE.

Kenjiro Nishikawa (A'93–M'99) was born in Nara, Japan, on September 18, 1965. He received the B.E. and M.E. degrees in welding engineering from Osaka University, Suita, Japan, in 1989 and 1991, respectively.

In 1991, he joined the NTT Radio Communication Systems Laboratories (now NTT Network Innovation Laboratories), Yokosuka, Japan, where he has been engaged in research and development on three-dimensional and uniplanar MMICs on Si and GaAs and their applications. His current interests are millimeter-wave communication systems and microwave/millimeter-wave photonics communication systems.

Mr. Nishikawa is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan. He was the recipient of the 1996 Young Engineer Award presented by the IEICE.